WHAT IS CLAIMED IS:

1. A MOS-gated transistor comprising:

a semiconductor substrate forming a collector region;

a drift region of a first conductivity type extending over the semiconductor substrate;

a first well region of a second conductivity type formed in an upper portion of the drift region, the first well region being coupled to an emitter terminal;

an impurity region of the first conductivity type formed in an upper portion of the drift region adjacent to the first well region so as to form a pn junction with the first well region, the impurity region having an impurity concentration higher than that of the drift region;

a floating well region of the second conductivity type formed in an upper portion of the drift region adjacent to the impurity region so as to form a pn junction with the impurity region, the floating well region being spaced apart from the first well region by the impurity region;

an emitter region formed in an upper portion of the first well region;

a gate insulating layer extending over a surface area of the first well region between the emitter region and the impurity region; and

a gate electrode extending over the gate insulating layer.

2. The MOS-gated transistor of claim 1 further comprising a buffer layer between the semiconductor substrate and the drift region and having the same conductivity type as the drift region.

3. The MOS-gated transistor of claim 2 wherein the buffer layer has a higher impurity concentration than the impurity region.

4. The MOS-gated transistor of claim 1 wherein a distance between the first well region and the floating well region is in a range of 3 μm to 6 μm.

5. The MOS-gated transistor of claim 1 wherein the thickness of the drift region is in a range of 40 μm to 120 μm.

6. The MOS-gated transistor of claim 1, wherein the semiconductor substrate has the first conductivity type.

7. The MOS-gated transistor of claim 1, wherein the semiconductor substrate has the second conductivity type.

8. The MOS-gated transistor of claim 1, wherein the emitter region has the first conductivity type.

9. A MOS-gated transistor comprising:

a semiconductor substrate coupled to a collector terminal;

an epitaxial layer of a first conductivity type extending over the semiconductor substrate;

a first well region of a second conductivity type formed in an upper portion of the epitaxial layer, the first well region being coupled to an emitter terminal;

an impurity region of the first conductivity type formed in an upper portion of the epitaxial layer adjacent to the first well region so as to form a first pn junction with the first well region;

a floating well region of the second conductivity type formed in an upper portion of the epitaxial layer adjacent to the impurity region so as to form a second pn junction with the impurity region, the floating well region being spaced apart from the first well region by the impurity region such that when the first and second pn junctions are reverse biased a boundary of a depletion region in the epitaxial layer is substantially flat;

an emitter region formed in an upper portion of the first well region; and

a gate terminal extending over but being insulated from a surface area of the first well region between the emitter region and the impurity region.

10. The MOS-gated transistor of claim 9 further comprising a buffer layer between the semiconductor substrate and the epitaxial layer and having the same conductivity type as the epitaxial layer.

11. The MOS-gated transistor of claim 10 wherein the buffer layer has a higher impurity concentration than the impurity region.

12. The MOS-gated transistor of claim 9 wherein a distance between the first well region and the floating well region is in a range of 3 μm to 6 μm.

13. The MOS-gated transistor of claim 9 wherein the thickness of the drift region is in a range of 40 μm to 120 μm.

14. A transistor comprising:

a semiconductor substrate forming a collector region;

a drift region of a first conductivity type extending over the semiconductor substrate; and

first and second well regions of a second conductivity each extending from an upper surface of the drift region into and terminating within the drift region, the first well region being coupled to an emitter terminal and the second well region floating, the first and second well regions being separated by an impurity region of the first conductivity type such that each of the first and second well regions forms a separate pn junction with the impurity region.

15. The transistor of claim 14 wherein the first and second well regions and the impurity region therebetween are configured such that when the separate pn junctions are reverse biased a boundary of a depletion region in the drift region is substantially flat.

16. The transistor of claim 14 wherein the impurity region has an impurity concentration higher than that of the drift region.

17. The transistor of claim 14 further comprising:

an emitter region of the first conductivity type formed in an upper portion of the first well region, the emitter region being coupled to the emitter terminal; and

a gate terminal extending over but being insulated from a surface area of the first well region between the emitter region and the impurity region.

18. The transistor of claim 14 further comprising a buffer layer between the semiconductor substrate and the drift region and having the same conductivity type as the drift region, the buffer layer having a higher impurity concentration than the impurity region.

19. The transistor of claim 14 wherein a distance between the first well region and the floating well region is in a range of 3 μm to 6 μm.

20. The transistor of claim 14 wherein the thickness of the drift region is in a range of 40 μm to 120 μm.

21. A MOS-gated transistor comprising:

a semiconductor substrate of a first conductivity type, forming a collector region;

a buffer layer of a second conductivity type extending over the semiconductor substrate;

a drift region of the second conductivity type extending over the semiconductor substrate;

a first well region of the first conductivity type formed in an upper portion of the drift region, the first well region being coupled to an emitter terminal;

an impurity region of the second conductivity type formed in an upper portion of the drift region adjacent to the first well region so as to form a first pn junction with the first well region, the impurity region having an impurity concentration higher than that of the drift region but lower than that of the buffer layer;

a floating well region of the second conductivity type formed in an upper portion of the drift region adjacent to the impurity region so as to form a second pn junction with the impurity region, the floating well region being spaced apart from the first well region by the impurity region such that when the first and second pn junctions are reverse biased a boundary of a depletion region in the epitaxial layer is substantially flat;

an emitter region of the first conductivity type formed in an upper portion of the first well region;

a gate insulating layer extending over a surface area of the first well region between the emitter region and the impurity region; and

a gate electrode extending over the gate insulating layer.

22. A method of forming a MOS-gated transistor comprising:

forming a drift region of a first conductivity type over a semiconductor substrate, the semiconductor substrate forming a collector region;

forming a first well region of a second conductivity type in an upper portion of the drift region; the first well region being coupled to an emitter electrode

forming an impurity region of the first conductivity type in an upper portion of the drift region adjacent to the first well region so as to form a pn junction with the first well region, the impurity region having an impurity concentration higher than that of the drift region;

forming a floating well region of the second conductivity type in an upper portion of the drift region adjacent to the impurity region so as to form a pn junction with the impurity region, the floating well region being spaced apart from the first well region by the impurity region;

forming an emitter region in an upper portion of the first well region;

forming a gate insulating layer extending over a surface area of the first well region between the emitter region and the impurity region; and

forming a gate electrode extending over the gate insulating layer.

23. The method of claim 22 further comprising forming a buffer layer over the semiconductor substrate before forming the drift region, the buffer layer having the same conductivity type as the drift region.

24. The method of claim 23 wherein the buffer layer has a higher impurity concentration than the impurity region.

25. The method of claim 22 wherein a distance between the first well region and the floating well region is in a range of 3 μm to 6 μm.

26. The method of claim 22 wherein the thickness of the drift region is in a range of 40 μm to 120 μm.

27. A method of forming a transistor, the method comprising:

forming a drift region of a first conductivity type over a semiconductor substrate, the semiconductor substrate forming a collector region;

forming a first well region of a second conductivity type extending from an upper surface of the drift region into and terminating within the drift region;

forming a second well region of the second conductivity extending from an upper surface of the drift region into and terminating within the drift region, the first well region being coupled to an emitter terminal and the second well region floating; and

forming an impurity region of the first conductivity type in the drift region between the first and second well regions so that each of the first and second well regions forms a separate pn junction with the impurity region.

28. The method of claim 27 wherein the first and second well regions and the impurity region therebetween are formed such that when the separate pn junctions are reverse biased a boundary of a depletion region in the drift region is substantially flat.

29. The method of claim 27 wherein the impurity region has an impurity concentration higher than that of the drift region.

30. The method of claim 27 further comprising:

forming an emitter region of the first conductivity type in an upper portion of the first well region, the emitter region being coupled to the emitter terminal; and

forming a gate terminal extending over but being insulated from a surface area of the first well region between the emitter region and the impurity region.

31. The method of claim 27 further comprising forming a buffer layer over the semiconductor substrate before forming the drift region, the buffer layer having the same conductivity type as the drift region, the buffer layer having a higher impurity concentration than the impurity region.